Claims:

1. An integrated circuit comprising:

a bipolar junction transistor in which a base contact region forms a fishbone configuration and an emitter region is adjacent to the periphery of said fishbone configuration.

2. The integrated circuit of claim 1, wherein an emitter contact region having an isomorphic shape with respect to said emitter region is in direct physical contact with the top surface of said emitter region.

3. The integrated circuit of claim 2, wherein said contact regions comprise a conductive material.

4. The integrated circuit of claim 3, wherein said conductive material comprises metal.

5. The integrated circuit of claim 1, wherein said bipolar junction transistor comprises at least one of the following semiconductor materials: Si, SiGe, GaAs, AlGaAs, InGaP, InP.

6. The integrated circuit of claim 1, wherein said bipolar junction transistor comprises a heterojunction bipolar transistor.

7. The integrated circuit of claim 6, wherein a base region contacting tab is embedded within an extension from a spine of said fishbone configuration.

8. The integrated circuit of claim 6, wherein said heterojunction bipolar transistor is employed in a linear power amplifier.

9. The integrated circuit of claim 8, wherein said linear power amplifier is employed in a cell phone.

10. The integrated circuit of claim 6, wherein said heterojunction bipolar transistor is employed in a saturated power amplifier.

11. The integrated circuit of claim 10, wherein said saturated power amplifier is employed in a cell phone.

12. The integrated circuit of claim 6, wherein said heterojunction bipolar transistor comprises at least one of the following pairs of semiconductor materials: AlGaAs/GaAs and InGaP/GaAs.

13. The integrated circuit of claim 7, wherein dimensions of at least one of the extensions from said spine of said fishbone configuration comprises: 10 microns in length by 1 micron in width.

14. The integrated circuit of claim 7, wherein the shortest distance between said base region and said emitter region comprises on the order of about 15 to 20 microns.

15. The integrated circuit of claim 7, wherein said fishbone configuration includes at least five extensions connected to said spine.

16. The integrated circuit of claim 7, wherein said fishbone configuration includes at least six extensions connected to said spine.

17. A device comprising:

a bipolar heterojunction transistor, said transistor having a collector-base capacitance (Ccb) and an extrinsic base resistance (Rb');

wherein said Ccb of said transistor is at least approximately 20 percent less than comparable interdigital BEB type bipolar heterojunction transistors and said Rb' is at least approximately 40 percent less than comparable interdigital EBE type bipolar heterojunction transistors.

18. The device of claim 17, wherein said Ccb of said transistor is at least approximately 25 percent less than comparable interdigital BEB type bipolar heterojunction transistors and said Rb' is at least approximately 50 percent less than comparable interdigital EBE type bipolar heterojunction transistors.

19. A method of manufacturing a bipolar junction transistor comprising:

forming an emitter contact region on the surface of the wafer;

removing the emitter material other than under said emitter contact region;

forming a base contact region adjacent to the periphery of the emitter contact region in a fishbone configuration;

forming a base mesa region including said emitter and base contact regions;

forming a collector contact region adjacent to the base mesa region; and

isolating said collector contact region and base mesa region from other devices.

20. The method of claim 19, and further comprising an ion implant to damage at least a portion of said base mesa.

21. The method of claim 20, wherein said ion implant comprises a multiple energy He ion implant to further reduce the collector-base capacitance.

22. The method of claim 19, wherein said contact regions comprise a conductive material.

23. The method of claim 19, wherein said bipolar junction transistor comprises at least one of the following semiconductor materials: Si, SiGe, GaAs, AlGaAs, InGaP, InP.

24. The method of claim 19, wherein said bipolar junction transistor comprises a heterojunction bipolar transistor.